

100V N-Ch Power MOSFET

Feature

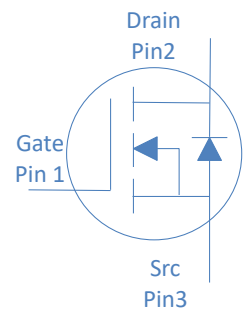
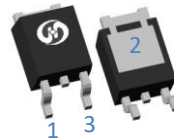
- ◇ High Speed Power Switching
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free

Application

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ Power Tools
- ◇ UPS
- ◇ Motor Control

| | | |
|-------------------------|-----|----|
| V_{DS} | 100 | V |
| $R_{DS(on),typ}$ | 22 | mΩ |
| I_D (Silicon Limited) | 31 | A |
| I_D (Package Limited) | 24 | A |

TO-252



| Part Number | Package | Marking |
|-------------|---------|-----------|
| HGD230N10A | TO-252 | GD230N10A |

Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ (unless otherwise specified)

| Parameter | Symbol | Conditions | Value | Unit |
|--|----------------|--|------------|------------------|
| Continuous Drain Current (Silicon Limited) | I_D | $T_C=25^\circ\text{C}$ | 31 | A |
| | | $T_C=100^\circ\text{C}$ | 22 | |
| | | $T_C=25^\circ\text{C}$ | 24 | |
| Continuous Drain Current (Package Limited) | | $T_C=25^\circ\text{C}$ | 24 | |
| Drain to Source Voltage | V_{DS} | - | 100 | V |
| Gate to Source Voltage | V_{GS} | - | ± 20 | V |
| Pulsed Drain Current | I_{DM} | - | 100 | A |
| Avalanche Energy, Single Pulse | E_{AS} | $L=0.4\text{mH}, T_C=25^\circ\text{C}$ | 20 | mJ |
| Power Dissipation | P_D | $T_C=25^\circ\text{C}$ | 52 | W |
| Operating and Storage Temperature | T_J, T_{stg} | - | -55 to 175 | $^\circ\text{C}$ |

Absolute Maximum Ratings

| Parameter | Symbol | Max | Unit |
|-------------------------------------|-----------------|-----|--------------------|
| Thermal Resistance Junction-Case | $R_{\theta JC}$ | 2.9 | $^\circ\text{C/W}$ |
| Thermal Resistance Junction-Ambient | $R_{\theta JA}$ | 50 | $^\circ\text{C/W}$ |

Electrical Characteristics at $T_j=25^\circ\text{C}$ (unless otherwise specified)
Static Characteristics

| Parameter | Symbol | Conditions | Value | | | Unit |
|-----------------------------------|---------------|---|-------|-----|-----------|-----------|
| | | | min | typ | max | |
| Drain to Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=250\mu A$ | 100 | - | - | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}=V_{DS}, I_D=250\mu A$ | 2 | 3 | 4 | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS}=0V, V_{DS}=100V, T_j=25^\circ\text{C}$ | - | - | 1 | μA |
| | | $V_{GS}=0V, V_{DS}=100V, T_j=100^\circ\text{C}$ | - | - | 100 | |
| Gate to Source Leakage Current | I_{GSS} | $V_{GS}=\pm 20V, V_{DS}=0V$ | - | - | ± 100 | nA |
| Drain to Source on Resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=10A$ | - | 22 | 25 | $m\Omega$ |
| Transconductance | g_{fs} | $V_{DS}=5V, I_D=10A$ | - | 19 | - | S |
| Gate Resistance | R_G | $V_{GS}=0V, V_{DS}$ Open, $f=1\text{MHz}$ | - | 1.7 | - | Ω |

Dynamic Characteristics

| | | | | | | |
|-------------------------------|--------------|--|---|-----|---|----|
| Input Capacitance | C_{iss} | $V_{GS}=0V, V_{DS}=50V, f=1\text{MHz}$ | - | 723 | - | pF |
| Output Capacitance | C_{oss} | | - | 107 | - | |
| Reverse Transfer Capacitance | C_{rss} | | - | 7.6 | - | |
| Total Gate Charge | Q_g | $V_{DD}=50V, I_D=10A, V_{GS}=10V$ | - | 11 | - | nC |
| Gate to Source Charge | Q_{gs} | | - | 3 | - | |
| Gate to Drain (Miller) Charge | Q_{gd} | | - | 3 | - | |
| Turn on Delay Time | $t_{d(on)}$ | $V_{DD}=50V, I_D=10A, V_{GS}=10V, R_G=10\Omega,$ | - | 6 | - | ns |
| Rise time | t_r | | - | 3 | - | |
| Turn off Delay Time | $t_{d(off)}$ | | - | 10 | - | |
| Fall Time | t_f | | - | 3 | - | |

Reverse Diode Characteristics

| | | | | | | |
|-------------------------|----------|--|---|-----|-----|----|
| Diode Forward Voltage | V_{SD} | $V_{GS}=0V, I_F=20A$ | - | 0.9 | 1.2 | V |
| Reverse Recovery Time | t_{rr} | $V_R=50V, I_F=10A, dI_F/dt=500A/\mu s$ | - | 33 | - | ns |
| Reverse Recovery Charge | Q_{rr} | | - | 132 | - | nC |

Fig 1. Typical Output Characteristics

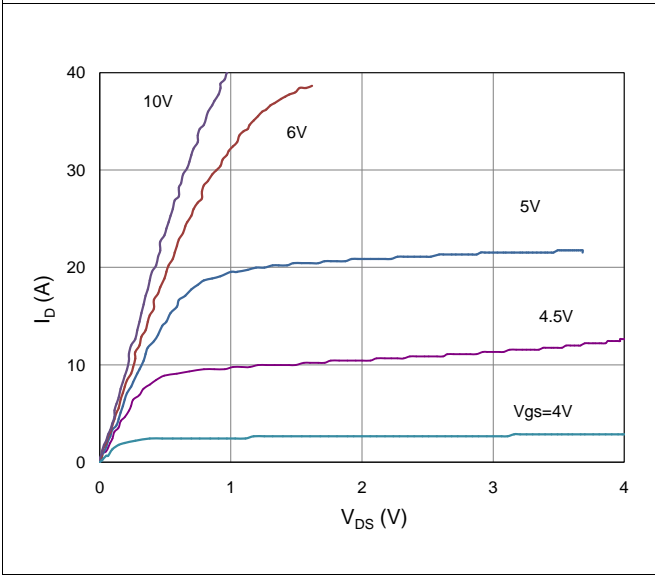


Figure 2. On-Resistance vs. Gate-Source Voltage

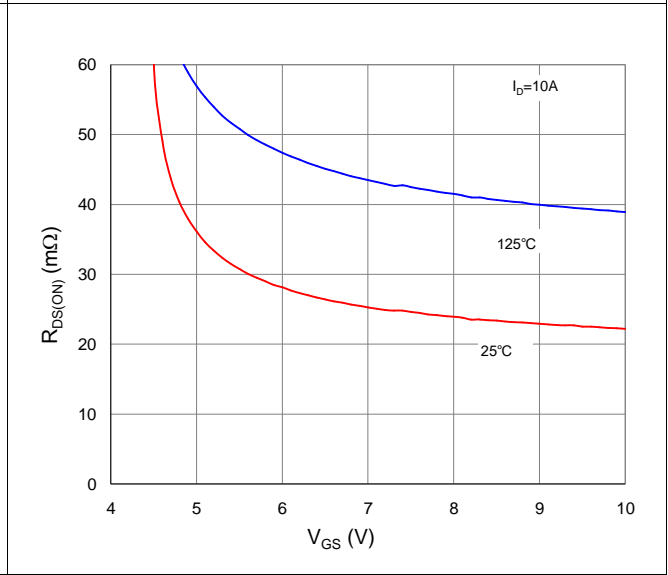


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

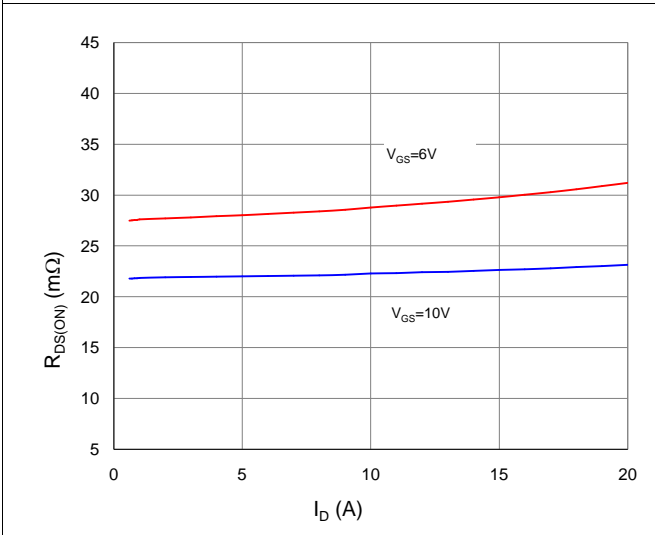


Figure 4. Normalized On-Resistance vs. Junction Temperature

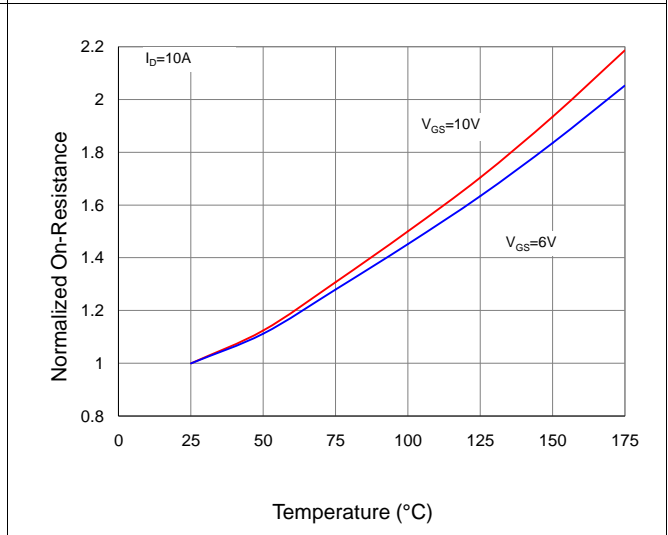


Figure 5. Typical Transfer Characteristics

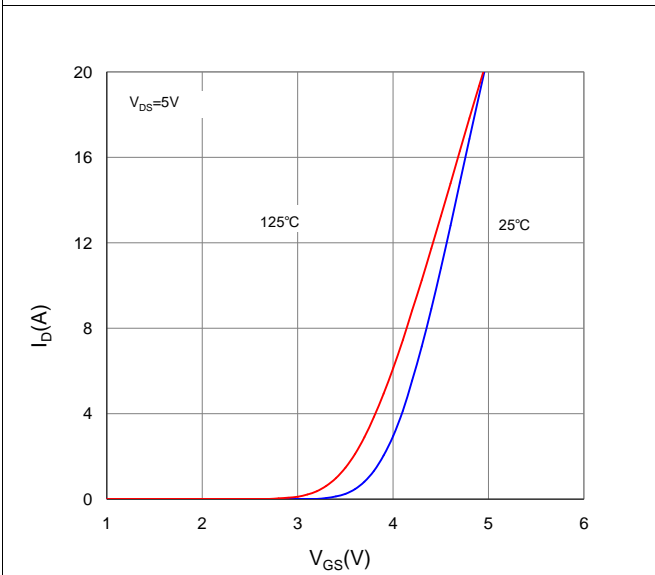


Figure 6. Typical Source-Drain Diode Forward Voltage

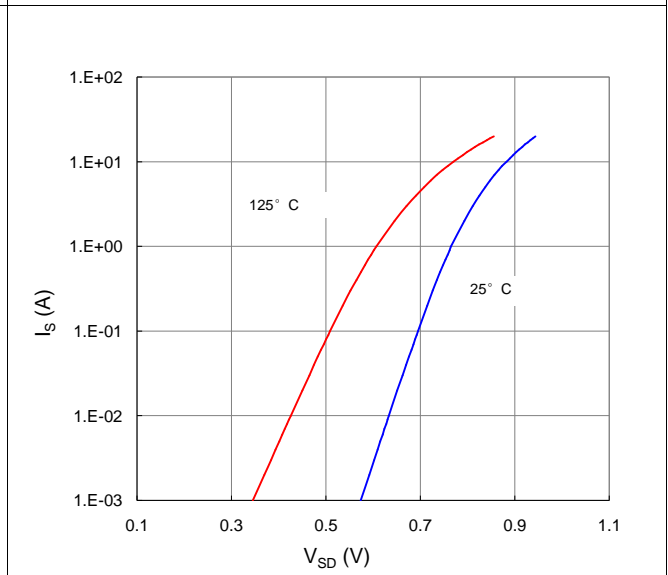


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

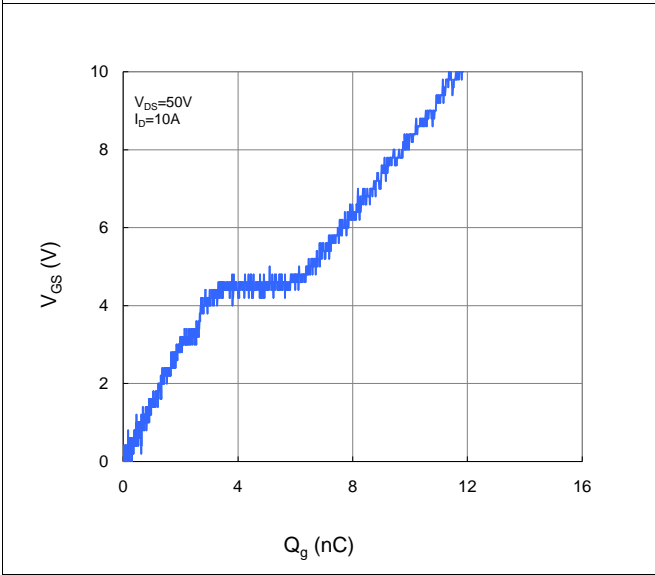


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

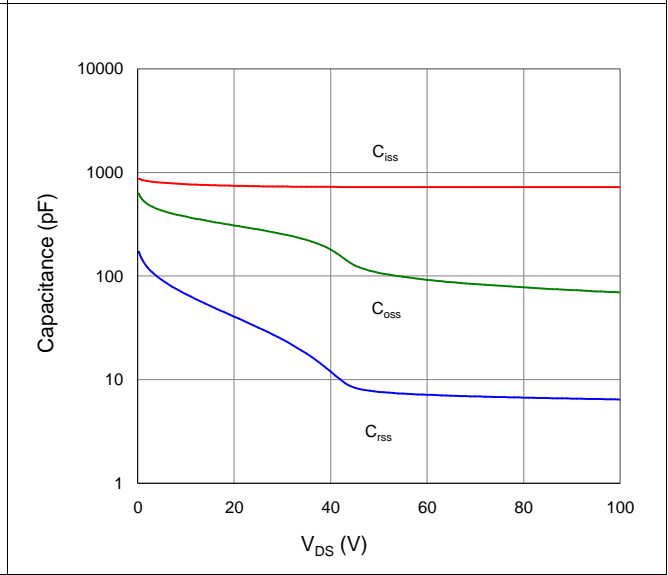


Figure 9. Maximum Safe Operating Area

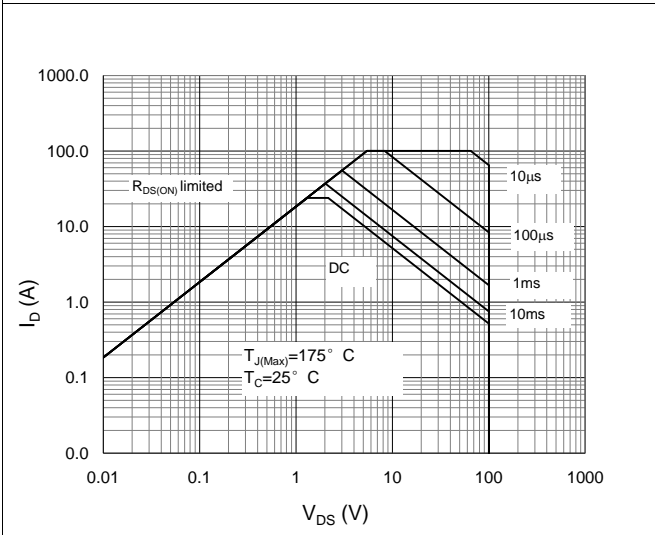


Figure 10. Maximum Drain Current vs. Case Temperature

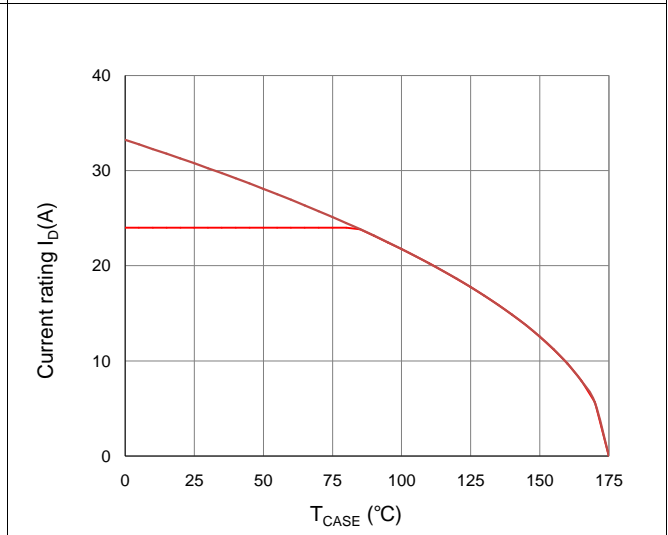
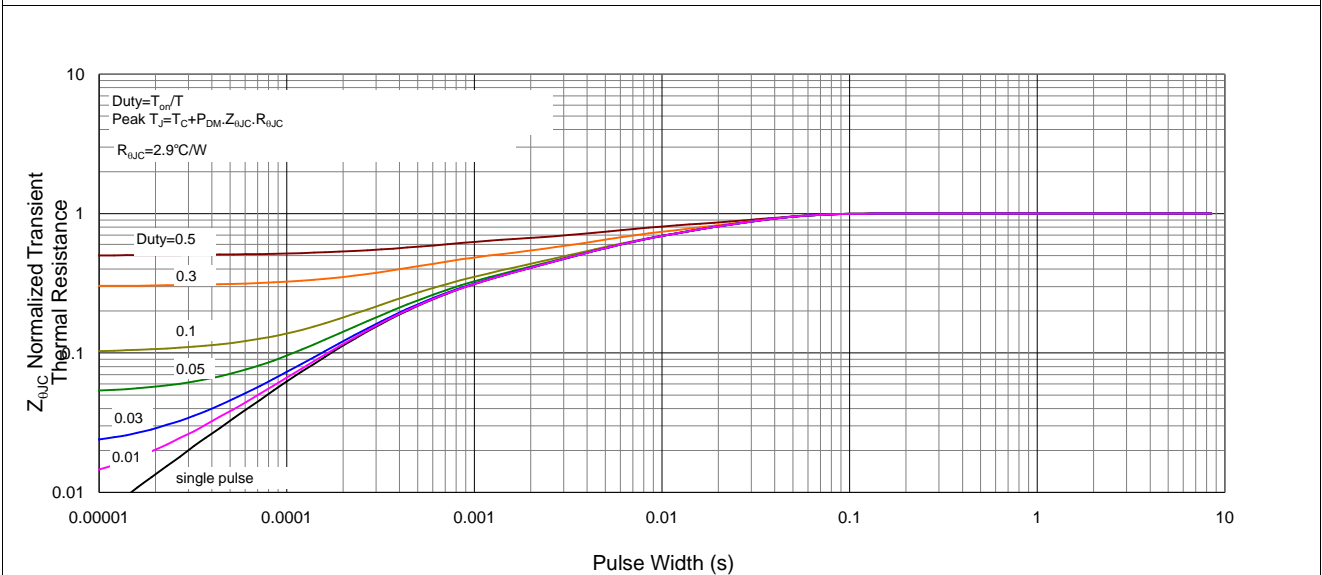
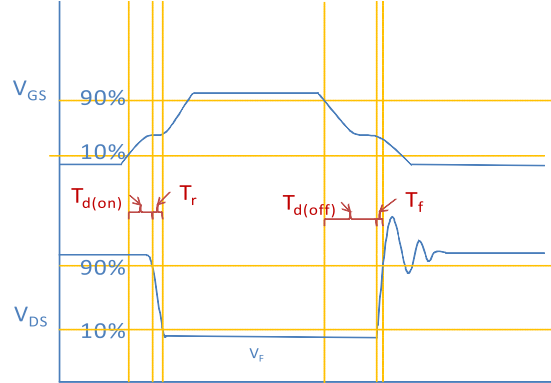
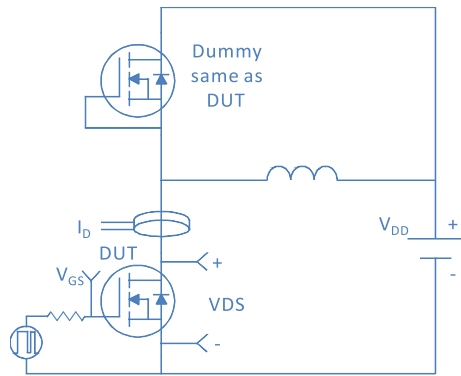


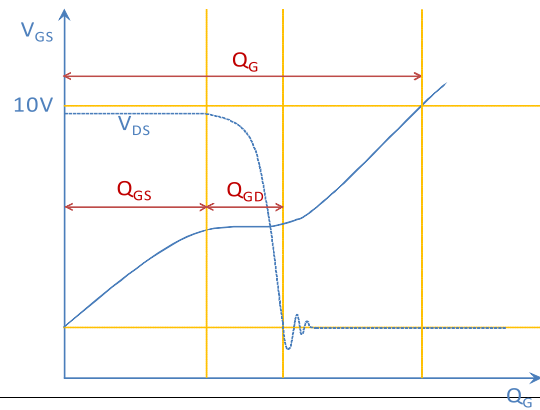
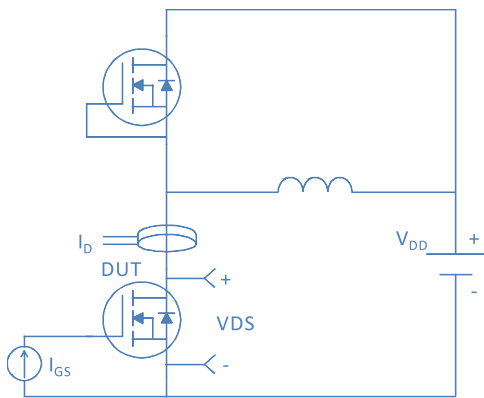
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



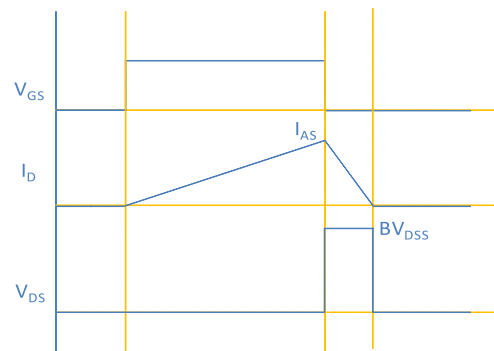
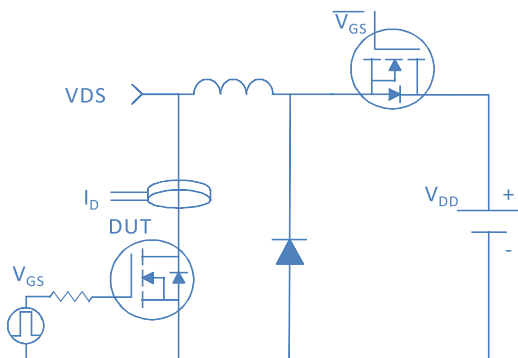
Inductive switching Test



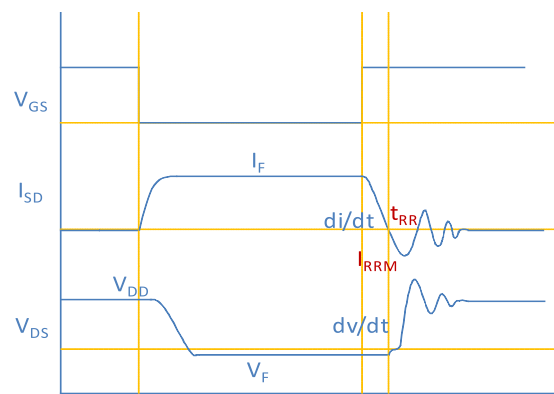
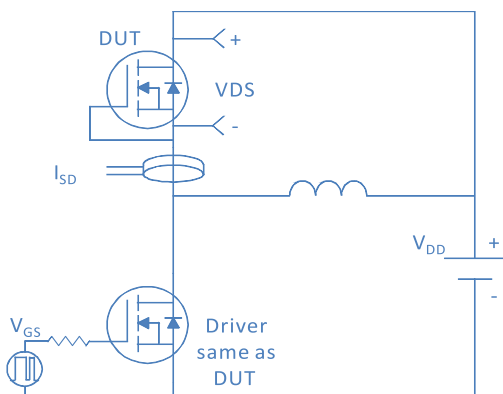
Gate Charge Test



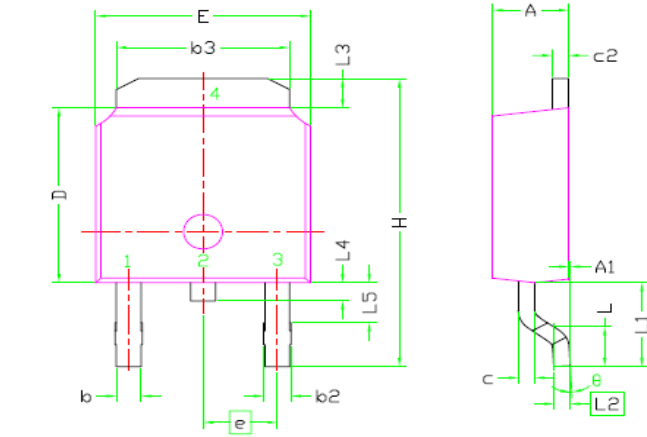
Unclamped Inductive Switching (UIS) Test



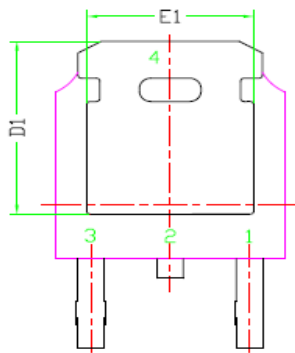
Diode Recovery Test



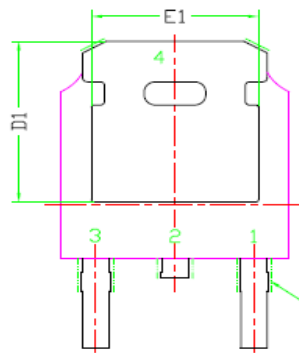
TO-252, 3 leads



| SYMBOL | DIMENSIONAL REQMTS | | |
|----------|--------------------|-------|-------|
| | MIN | NOM | MAX |
| E | 6.40 | 6.60 | 6.731 |
| L | 1.40 | 1.52 | 1.77 |
| L1 | 2.743 REF | | |
| L2 | 0.508 BSC | | |
| L3 | 0.89 | -- | 1.27 |
| L4 | 0.64 | -- | 1.01 |
| L5 | -- | -- | -- |
| D | 6.00 | 6.10 | 6.223 |
| H | 9.40 | 10.00 | 10.40 |
| b | 0.64 | 0.76 | 0.88 |
| b2 | 0.77 | 0.84 | 1.14 |
| b3 | 5.21 | 5.34 | 5.46 |
| e | 2.286 BSC | | |
| A | 2.20 | 2.30 | 2.38 |
| A1 | 0 | -- | 0.127 |
| c | 0.46 | 0.50 | 0.60 |
| c2 | 0.46 | 0.50 | 0.58 |
| D1 | 5.21 | -- | -- |
| E1 | 4.40 | -- | -- |
| θ | 0° | -- | 10° |



SINGLE ROW<NEW>



MATRIX L/F

COPPER EXPOSITION AREA